LCD Module User Manual

EDM 640240-01

REVISION RECORD		
REV. NO.	DATA	REVISION ITEMS
1.0	2 , 7, 2007	First Release Version

Contents

1.Scope

This manual defines general provisions as well as inspection standards for standard LCD module. If the event of unforeseen problem or unspecified items may occur, please contact the nearest supplier or our company.

2.Warranty

If module is not stored or used as specified in this manual, it will be void the 12- month warranty.

3.Features

3-1. Features

(1) Display mode: Transflactive/positive
FSTN LCD

(2) Display color: Display dots: Black
Background : White

（3）Display Format: 640(w)×240(h) full dots

(4) Input data: 8-bit parallel data interfaced from a MPU

(5) Multiplex ratio: 1/240 Duty, 1/16Bias

（6）Viewing direction: 6 O'clock

(7) Back light : LED White

(8) Controller: SID13700

3-2. Mechanical features

Item	Specifications	Unit
Outline dimensions	180.0(W)×80.0(H) ×12.5Max.(T)	mm
Viewing Area	155.0(W)×60.0(H)	mm
Image Area	153.59(W)×57.59(H)	mm
Number of Dots	640 (W)×240(H)	---
Dot Size	0.225(W)×0.225(H)	mm
Dot Pitch	0.24(W)×0.24(H)	mm

3-3. Absolute maximum ratings

Item	Symbol	Condition	Min	Max	Units
Power supply for logic	HVdd	25℃	-0.3	7.0	V
	LVdd	25℃	-0.3	4.0	
Input voltage	HVin	25℃	-0.3	HVdd+0.5	V
	LVin	25℃	-0.3	LVdd+0.5	
Output voltage	HVout	25℃	-0.3	HVdd+0.5	V
	LVout	25℃	-0.3	LVdd+0.5	
Operating temperature	Top	---	-40	80	℃
Storage temperature	Tstg	---	- 65	150	℃

NOTE:

(1) When using a power supply with high impedance,a large potential difference between the chip's internal power supply voltage and the input voltage may occur,thus making the power supply susceptible to latch-up.Therefore,pay particular attention to the power supply and its wiring.

(2) All voltage are based on Vss=0.

(3) The symbol H***indicates 5V-block pins;L*** indicates 3.3V-block pins

3-4Electrical Characteristics

[V_{SS} = 0V, HV_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	—	-1	—	1	uA
OFF-state Leakage Current	I_{OZ}	—Note 2)	-1	—	1	uA
High Level Output Voltage	V_{OH}	I_{OH} = -8.0mA HV_{DD}=Min	HV_{DD}-0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 8.0m HV_{DD}=Min	—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS level HV_{DD} = Max	3.5	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS level HV_{DD} = Min	—	—	1.0	V
Positive Trigger Voltage	V_{T1+}	CMOS Schmitt	2.0	—	4.0	V
Negative Trigger Voltage	V_{T1-}	CMOS Schmitt	0.8	—	3.1	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt	0.3	—	—	V
High Level Input Voltage	V_{IH2}	TTL level HV_{DD} = Max	2.0	—	—	V
Low Level Input Voltage	V_{IL2}	TTL level HV_{DD} = Min	—	—	0.8	V
Pulldown Resistance	R_{PD}	VI = HV_{DD}	30	60	144	kΩ
Operating Supply Current	I_{opr}	f_{OSC} =10 MHz Nonloaded 256 x 200dot	—	TBD	TBD	mA
Quiescent Supply Current (between HV_{DD} and V_{SS})	I_{QH}	Sleep mode XCG1, CS#, $\overline{RD}$# = V_{DD}	—	—	30	uA
Quiescent Supply Current (between LV_{DD} and V_{SS})	I_{QH}	Sleep mode XCG1, CS#, $\overline{RD}$# = V_{DD}	—	—	35	uA

Note: 1. The pulse applied to the RESET# pin must be held low for 200 μs or more to be effective. However, avoid keeping the input pulse active for more than several seconds because the LCD's d.c. drive capability may be adversely affected.

2. The VB0–DB7 pins come with a feedback circuit, so that even when input becomes high impedance, the pins retain the state held immediately before. Therefore, input voltage of an intermediate level allows input current to flow to the pin.

[V_{SS} = 0V, VDD = LV_{DD} = 3.3 – 0.3V, Ta = -40 – 85°C]

Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	—	-1	—	1	uA
OFF-state Leakage Current	I_{OZ}	— Note 2)	-1	—	1	uA
High Level Output Voltage	V_{OH}	I_{OH} = -6.0mA HV_{DD}=Min	HV_{DD}-0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 6.0m HV_{DD}=Min	—	—	0.4	V
High Level Input Voltage	V_{IH1}	LVTTL level V_{DD} = Max	2.0	—	—	V
Low Level Input Voltage	V_{IL1}	LVTTL level V_{DD} = Min	—	—	0.8	V
Positive Trigger Voltage	V_{T1+}	LVTTL Schmitt	1.1	—	2.4	V
Negative Trigger Voltage	V_{T1-}	LVTTL Schmitt	0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	LVTTL Schmitt	0.1	—	—	V
Pulldown Resistance	R_{PD}	VI = V_{DD}	20	50	120	kΩ
Operating Supply Current	I_{opr}	f_{OSC} =10 MHz Nonloaded 256 x 200dot	—	TBD	TBD	mA
Quiescent Supply Current (between LV_{DD} and V_{SS})	I_{QH}	Sleep mode XCG1, CS#, RD# = V_{DD}	—	—	35	uA

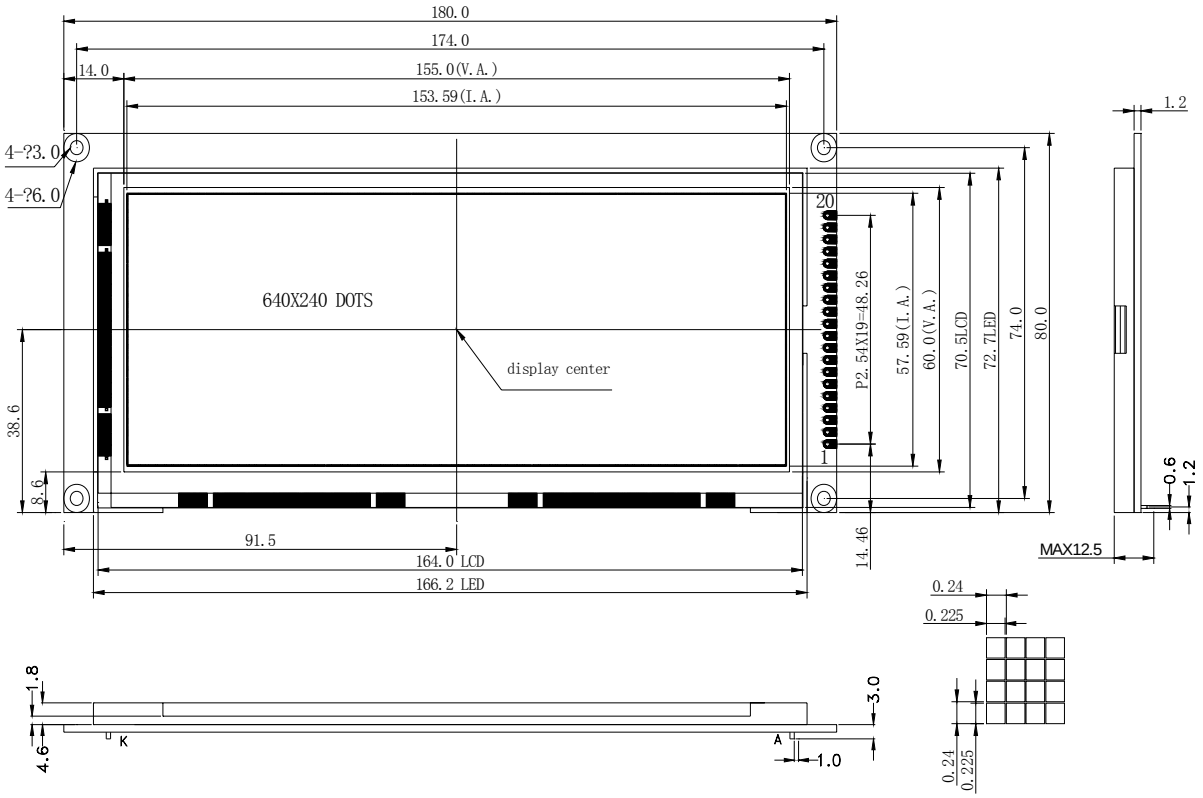
3-5 Electro-optical Characteristics

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
LCD Driving Voltage (Recommended voltage)		Vop	-20℃	---	---	---	V
			25℃	---	18.4	---	
			70℃	---	---	---	
Current consumption(No B/L)	logic	Idd	Vdd=5V Fflm=75Hz	—	500	700	uA
				—	200	250	
	LCD drive	Iee		—	540	810	
				—	250	300	
Power supply for logic		Vdd-Vss	25℃	2.7	—	5.5	V

3-6 LED back light specifications

Item	Unit	Standard Values			Condition
		Min.	Typ.	Max.	
Supply Voltage	V	—	3.2	---	—
Current	mA	---	150	---	---
Luminous Color	—	W hite			---
Operating Temp.	℃	-20 ~ +70			—
Storage Temp.	℃	-30 ~ +80			—

4. Mechanical Diagram



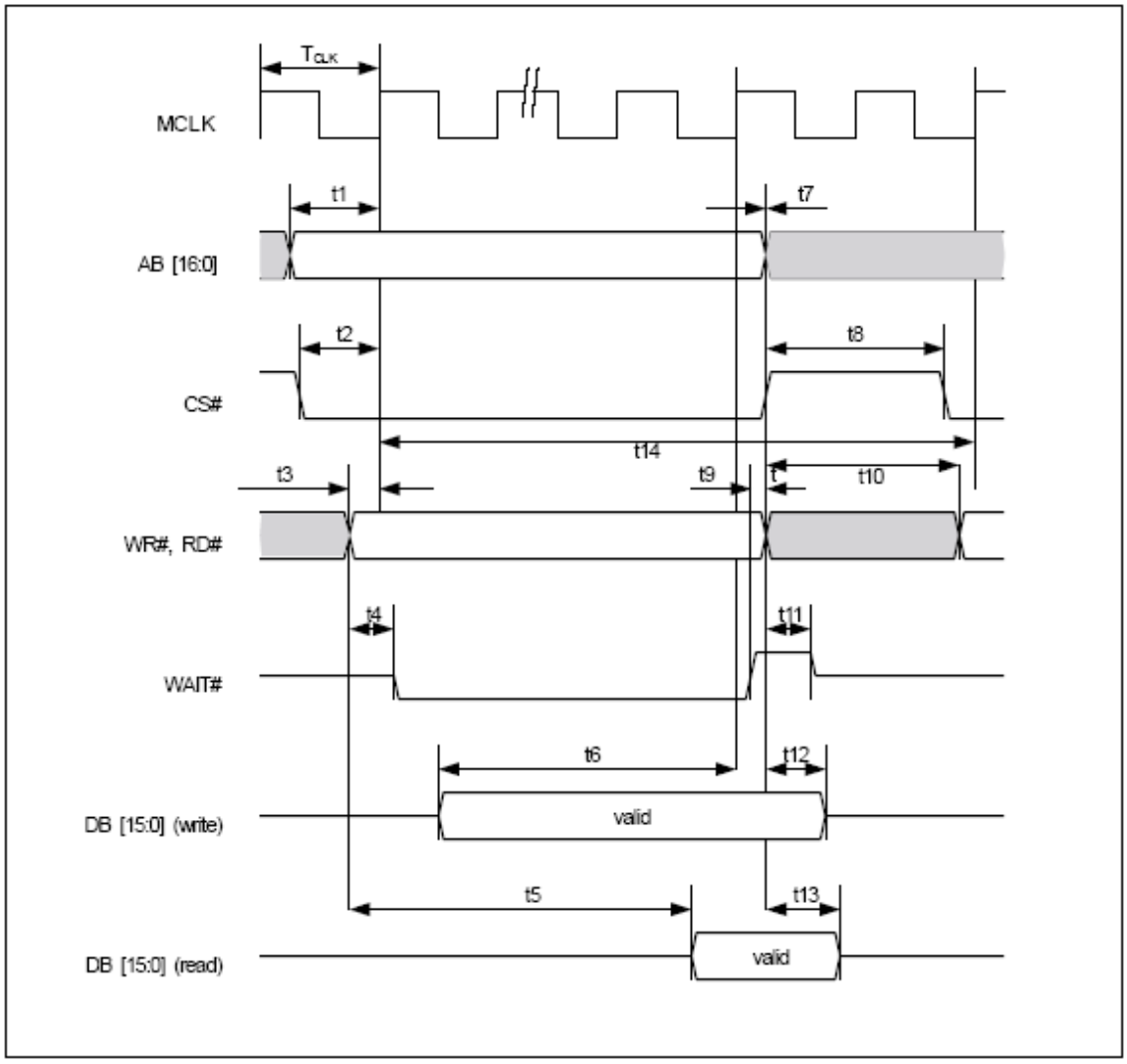
5.I/O Terminal

5-1 I/O Connection

Pin No.	Symbol	Function
1	Vss	GND
2	Vdd	POWER SUPPLY FOR LOGIC
3	V0	DRIVING VOLTAGE FOR LCD
4	A0	DATA TYPE SELECT
5	/WR	8080:WRITE SIGNAL 6800:R/W SIGNAL
6	/RD	8080:READ SIGNAL 6800:ENABLE SIGNAL
7-14	DB0-DB7	DATA BUS LINE
15	/CS	CHIP SELECT,ACTIVEL
16	/RES	CONTROLLER RESET SIGNAL
17	VEE	NEGATIVE VOLTAGE OUTPUT
18	CNF3	H:6800 L:8080
19	LED+	BACKLIGHT VOLTAGE+
20	LED-	BACKLIGHT VOLTAGE-

5-2 Signal timing diagram

5-2-1 8080 family interface Timing



* MCLK denotes CLKI or the internally generated system clock.

Gemeric Bus Interface Timing

[V_{SS} = 0V, V_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

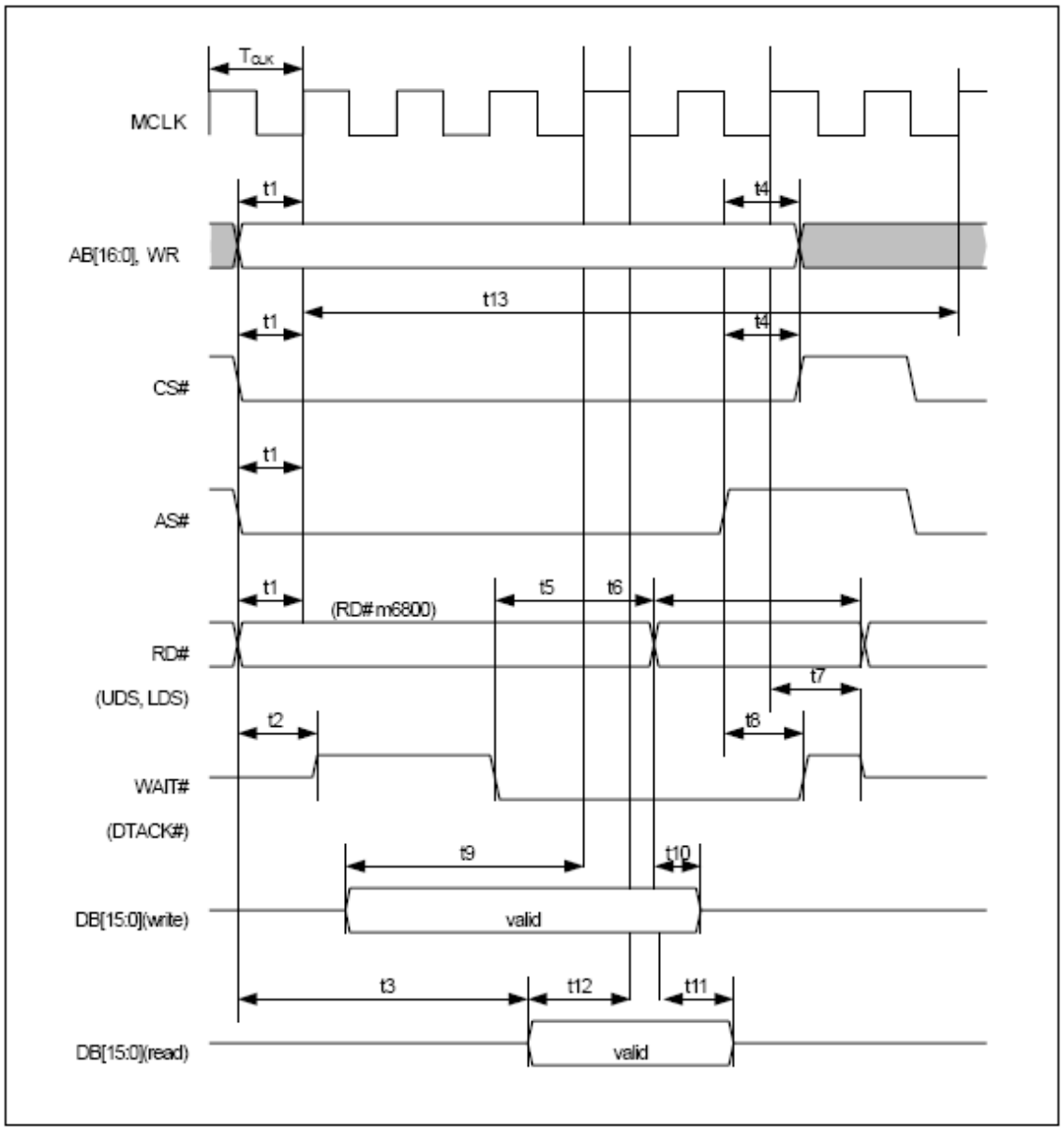
Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	1/f_{CLK}	—	ns
t1	AB [16 : 0] setup to first CLK rising edge where CS# = 0 and either RD# = 0 or WR# = 0	11	—	ns
t2	CS# setup to CLK rising edge	9	—	ns
t3	RD#, WR# setup to CLK rising edge	9	—	ns
t4	RD#, WR# state change to WAIT# driven low	1	5	ns
t5	RD# falling edge to DB [15 : 0] driven (ead cycle)	3Tc+9ns	—	Tclk
t6	DB [15 : 0] setup to 4th rising CLK edge after CS# = 0 and WR# = 0	1	—	T_{CLK}
t7	AB [16 : 0], CS# hold from RD#, WR# rising edge	8	—	ns
t8	CS# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t9	WAIT# rising edge to RD#, WR# rising edge	0	—	ns
t10	WR#, RD# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t11	Rising edge of either RD# or WR# to WAIT# high impedance 0.5 TCLK	—	0.5	T_{CLK}
t12	D [15 : 0] hold from WR# rising edge (write cycle)	1	—	ns
t13	D [15 : 0] hold from RD# rising edge (read cycle)	1	—	ns
t14	Cycle Length Read Write (next write cycle) Write (next read cycle)	6 7 10	—	T_{CLK}

Gemeric Bus Interface Timing

[V_{SS} = 0V, V_{DD} = 3.0 – 3.6V, Ta = -40 – 85°C]

Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	1/f_{CLK}	—	ns
t1	AB [16 : 0] setup to first CLK rising edge where CS# = 0 and either RD# = 0 or WR# = 0	12	—	ns
t2	CS# setup to CLK rising edge	11	—	ns
t3	RD#, WR# setup to CLK rising edge	11	—	ns
t4	RD#, WR# state change to WAIT# driven low	1	7	ns
t5	RD# falling edge to DB [15 : 0] driven (ead cycle)	3Tc+11ns	—	Tclk
t6	DB [15 : 0] setup to 4th rising CLK edge after CS# = 0 and WR# = 0	1	—	T_{CLK}
t7	AB [16 : 0], CS# hold from RD#, WR# rising edge	10	—	ns
t8	CS# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+10ns 5Tclk+10ns	—	 ns ns ns
t9	WAIT# rising edge to RD#, WR# rising edge	0	—	ns
t10	WR#, RD# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+10ns 5Tclk+10ns	—	 ns ns ns
t11	Rising edge of either RD# or WR# to WAIT# high impedance 0.5 TCLK	—	0.5	T_{CLK}
t12	D [15 : 0] hold from WR# rising edge (write cycle)	1	—	ns
t13	D [15 : 0] hold from RD# rising edge (read cycle)	1	—	ns
t14	Cycle Length Read Write (next write cycle) Write (next read cycle)	6 7 10	—	T_{CLK}

5-2-2 *System Bus Read/write characteristics II (MC68K-series MPU)*



* MCLK denotes CLKI or the internally generated system clock.

Motorola M68K#1 Interface Timing

[V_{SS} = 0V, V_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

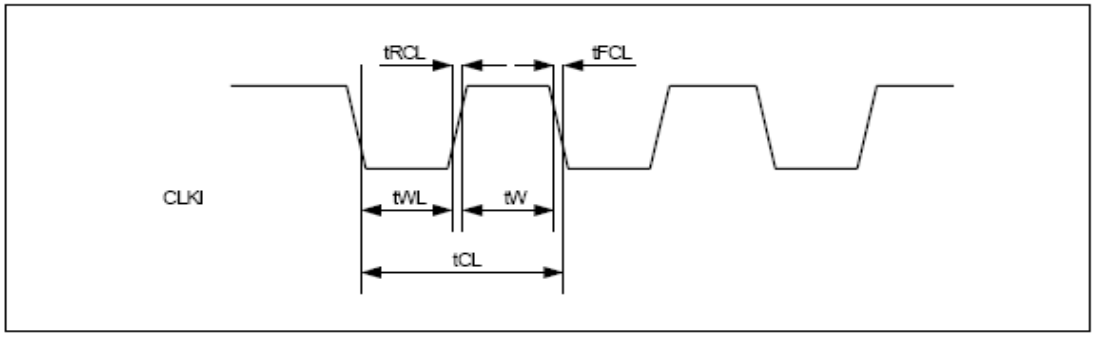
Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	$1/f_{CLK}$	—	ns
t1	AB [16 : 0], WR# (R/W#) and CS# and AS# and RD# (UDS#, LDS#) setup to first CLK rising edge	9	—	ns
t2	CS# and AS# asserted to WAIT# (DTACK#) driven	1	7	ns
t3	RD# = 0 (UDS# = 0 or LDS# = 0) to DB [15 : 0] driven (read cycle)	3Tclk+9ns	—	ns
t4	AB [16 : 0], WR# (R/W#) and CS# hold from AS# rising edge	0	—	ns
t5	WAIT# (DTACK#) falling edge to RD# (UDS#, LDS#) rising edge	1	—	T_{CLK}
t6	RD# (USD#, LDS#) deasserted high to reasserted low - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t7	CLK rising edge to WAIT# (DTACK#) high impedance	—	$1T_{CLK}$-2	ns
t8	AS# rising edge to WAIT# (DTACK#) rising edge	3	12	ns
t9	DB [15 : 0] valid to 4th CLK rising edge where CS# = 0, AS# = 0 and either RD# = 0 (UDS# = 0 or LDS# = 0) (wirte cycle)	1	—	T_{CLK}
t10	DB [15 : 0] hold from RD# (UDS#, LDS#) falling edge (wirte cycle)	4	—	ns
t11	RD# (UDS#, LDS#) rising edge to DB [15 : 0] high impedance (read cycle)	6	—	ns
t12	DB [15 : 0] valid setup time to 2nd CLK falling edge after WAIT# (DTACK#) goes low (read cycle)	6	—	ns
t13	t13 Cycle Length Read Write (next write cycle) Write (next read cycle)	7 8 11	—	T_{CLK}

Motorola M68K#1 Interface Timing

[V_{SS} = 0V, V_{DD} = 3.0 – 3.6V, Ta = -40 – 85°C]

Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	$1/f_{CLK}$	—	ns
t1	AB [16 : 0], WR# (R/W#) and CS# and AS# and RD# (UDS#, LDS#) setup to first CLK rising edge	9	—	ns
t2	CS# and AS# asserted to WAIT# (DTACK#) driven	1	10	ns
t3	RD# = 0 (UDS# = 0 or LDS# = 0) to DB [15 : 0] driven (read cycle)	3Tclk+9ns	—	ns
t4	AB [16 : 0], WR# (R/W#) and CS# hold from AS# rising edge	0	—	ns
t5	WAIT# (DTACK#) falling edge to RD# (UDS#, LDS#) rising edge	1	—	T_{CLK}
t6	RD# (UDS#, LDS#) deasserted high to reasserted low - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t7	CLK rising edge to WAIT# (DTACK#) high impedance	—	$1T_{CLK}$-2	ns
t8	AS# rising edge to WAIT# (DTACK#) rising edge	3	15	ns
t9	DB [15 : 0] valid to 4th CLK rising edge where CS# = 0, AS# = 0 and either RD# = 0 (UDS# = 0 or LDS# = 0) (wirte cycle)	1	—	T_{CLK}
t10	DB [15 : 0] hold from RD# (UDS#, LDS#) falling edge (wirte cycle)	4	—	ns
t11	RD# (UDS#, LDS#) rising edge to DB [15 : 0] high impedance (read cycle)	8	—	ns
t12	DB [15 : 0] valid setup time to 2nd CLK falling edge after WAIT# (DTACK#) goes low (read cycle)	8	—	ns
t13	Cycle Length Read Write (next write cycle) Write (next read cycle)	7 8 11	—	T_{CLK}

5-2-3 *External Clock Input Characteristics*



[V_{SS} = 0V, V_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

Symbol	Parameter			Unit
		Min.	Max.	
t_{RCL}	External input clock rise time	—	2	ns
t_{FCL}	External input clock fall time	—	2	ns
t_{WH}	High-level pulse width of external input clock	7	—	ns
t_{WL}	Low-level pulse width of external input clock	7	—	ns
t_{CL}	External input clock period	16.4	—	ns

5-3 MPU INTERFACE

The S1D13700 uses a combination of CNF2/3/4, AB15–0, RD#, WR#, and CS# to discriminate information supplied to it via the system data bus as described in Section 2.2 "Pin Functions" on page 9.

In indirect interface mode, AB0 generally is connected to the least significant bit of the system address bus. CNF2 and CNF3 are provided for changing the functions of S1D13700 pins 58 and 59 to enable the chip to be connected directly to the 80 or 68-series MPU bus, and are pulled high or low through a resistor when in use. For the 80-series MPU, the S1D13700 should normally be mapped in I/O space.

5-3-1 80-series MPU

<Direct access for the 80-series interface>

CNF4	AB15 – AB1	AB0	RD#	WR#	Function
0	0or1	0or1	0	1	Read from command/parameter registers
0	0or1	0or1	1	1	Write to command/parameter registers

<Indirect access for the 80-series interface>

CNF4	AB15 – AB1	AB0	RD#	WR#	Function
1	—	0	0	1	—
1	—	1	0	1	Data (display data and cursor address) read
1	—	0	1	0	Data (display data and parameter) write
1	—	1	1	0	Command write (code only)

5-3-2 68-series MPU

<Direct access for the 68-series interface>

CNF4	AB15 – AB1	AB0	WR# (R/W#)	RD# (E)	Function
0	0or1	0or1	1	1	Read from command/parameter registers
0	0or1	0or1	0	1	Write to command/parameter registers

<Indirect access for the 68-series interface>

CNF4	AB15 – AB1	AB0	WR# (R/W#)	RD# (E)	Function
1	—	0	1	1	—
1	—	1	1	1	Data (display data and cursor address) read
1	—	0	0	1	Data (display data and parameter) write
1	—	1	0	1	Command write (code only)

5-4 display command

When indirect mode is selected for the system interface, use commands to set up the display.

The table below lists the types of commands, including the code of each command.

Purpose	Command	Code										Command description	Parameters following the command		Remarks
		WR#	RD#	AB0	DB BIN 7	6	5	4	3	2	1	0	DB HEX		No. of parameters	See pages	
Operation control	SYSTM SET	1	0	1	0	1	0	0	0	0	0	0	40	Sets initial operation and window size.	8	19	
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Sleep operation.	0	27	Note 1
Display control	DISPON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 • 59	Instructs to turn display on or off and make the screen flash on and off.	1	28	Note 1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Sets the display start address and display area.	10	29	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Sets the cursor shape, etc.	2	37	
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C – 4F	Sets the direction of cursor movement.	0	38	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Instructs screen overlay mode.	1	39	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Sets the start address of CG RAM.	2	43	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Sets the horizontal direction dot unit and scroll position.	1	44	
	GRAY SCALE	1	0	1	0	1	1	0	0	0	0	0	60	Sets grayscale mode.	0	45	
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Sets the cursor address.	2	45	Note 1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Instructs to read the cursor address.	2	46	Note 1
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Instructs to write to display memory.	—	47	Note 1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Instructs to read display memory data.	—	47	

Note 1: As a rule, each command is executed every time a parameter for the command is input to the S1D13700, and completed before the next parameter (P) or command (C) is input. Therefore, the MPU can stop sending parameters in the middle and send the next command.

6. Quality Level

6-1 Inspection conditions

6-1-1The environmental conditions for inspection shall be as follows:

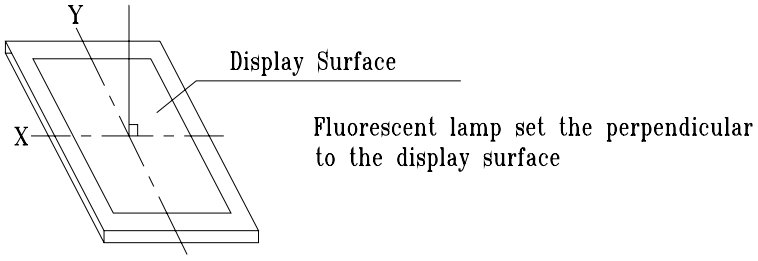
Room temperature: 20±3℃

Humidity: 65±20% RH

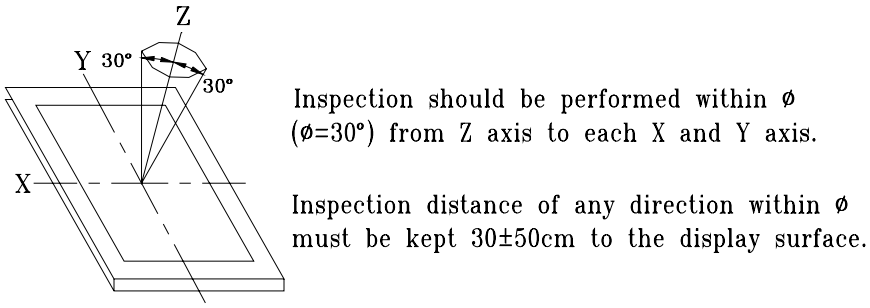
6-1-2 The external visual inspection:

The inspection shall be performed by using a 20W fluorescent lamp for illumination and the distance between LCD and the eyes of the inspector should be at least 30cm.

(1) Light method



(2) Inspection distance and angle



6-2 Sampling procedures for each item's acceptance level table

Defect type	Sampling procedure	AQL
Major defect	MIL-STD-105D Inspection Level I Normal inspection Single sample inspection	Q/DF-01-06
Minor defect	MIL-STD-105D Inspection Level I Normal inspection Single sample inspection	Q/DF-01-06

6-3 Classification of defects

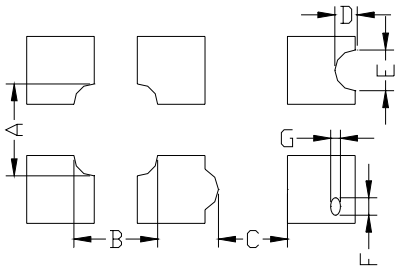
6-3-1 Major defect

A major defect refers to a defect that may substantially degrade usability for product applications.

6-3-2 Minor defect

A minor defect refers to a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation.

6-4 Inspection standar

<table>
<tr><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1) Display on inspection</td><td>(1) Non display (2) Vertical line is deficient
(3) Horizontal line is deficient (4) Cross line is deficient</td><td>Major</td></tr>
<tr><td>2) Black / White spot</td><td>
<table>
<tr><th>Size Φ(mm)</th><th>Acceptable number</th></tr>
<tr><td>Φ≤0.3</td><td>Ignore (note)</td></tr>
<tr><td>0.3<Φ≤0.45</td><td>3</td></tr>
<tr><td>0.45<Φ≤0.6</td><td>1</td></tr>
<tr><td>0.3<Φ</td><td>0</td></tr>
</table>
(Note) Not allowed if four more spots crowd together</td><td>Minor</td></tr>
<tr><td>3) Black / White line</td><td>
<table>
<tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr>
<tr><td>L≤10</td><td>W≤0.03</td><td>Ignore</td></tr>
<tr><td>5.0≤L≤10</td><td>0.03<W≤0.04</td><td>3</td></tr>
<tr><td>5.0≤L≤10</td><td>0.04<W≤0.05</td><td>2</td></tr>
<tr><td>1.0≤L≤10</td><td>0.05<W≤0.06</td><td>2</td></tr>
<tr><td>1.0≤L≤10</td><td>0.06<W≤0.08</td><td>1</td></tr>
<tr><td>L≤10</td><td>0.08<W</td><td>follows 2) point defect</td></tr>
</table>
Defects separate with each other at an interval of more than 20mm.</td><td>Minor</td></tr>
<tr><td>4) Display pattern</td><td> 

[Unit: mm]
<table>
<tr><th>A+B≤0.45</th><th>0<C</th><th>D+E≤0.35</th><th>F+G≤0.35</th></tr>
<tr><td>2</td><td></td><td>2</td><td>2</td></tr>
</table>
Note: 1) Up to 3 damages acceptable
2) Not allowed if there are two or more pinholes every 3 of fourths inch.</td><td>Minor</td></tr>
<tr><td>5) Spot-like contrast irregularity</td><td>
<table>
<tr><th>Size Φ(mm)</th><th>Acceptable Number</th></tr>
<tr><td>Φ≤0.7</td><td>Ignore (note)</td></tr>
<tr><td>0.7<Φ≤1.0</td><td>3</td></tr>
<tr><td>1.0<Φ≤1.5</td><td>1</td></tr>
<tr><td>1.5<Φ</td><td>0</td></tr>
</table>
Note: 1) Conformed to limit samples.
2)Intervals of defects are more than 30mm.</td><td>Minor</td></tr>
</table>

<table>
<tr><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>6) Bubbles in polarizer</td><td><table><tr><th>Size Φ(mm)</th><th>Acceptable Number</th></tr><tr><td>Φ≤0.4</td><td>Ignore (note)</td></tr><tr><td>0.4<Φ≤0.65</td><td>2</td></tr><tr><td>0.65<Φ≤1.2</td><td>1</td></tr><tr><td>1.2<Φ</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>7) Scratches and dent on the polarizer</td><td>Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.</td><td>Minor</td></tr>
<tr><td>8) Stains on the surface of LCD panel</td><td>Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.</td><td>Minor</td></tr>
<tr><td>9) Rainbow color</td><td>No rainbow color is allowed in the optimum contrast on state within the active area.</td><td>Minor</td></tr>
<tr><td>10) Viewing area encroachment</td><td>Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.</td><td>Minor</td></tr>
<tr><td>11) Bezel appearance</td><td>Rust and deep damages that are visible in the bezel are rejected.</td><td>Minor</td></tr>
<tr><td>12) Defect of land surface contact</td><td>Evident crevices that are visible are rejected.</td><td>Minor</td></tr>
<tr><td>13) Parts mounting</td><td>(1) Failure to mount parts
(2) Parts not in the specifications are mounted
(3) For example: Polarity is reversed, HSC or TCP falls off.</td><td>Major</td></tr>
<tr><td>14) Part alignment</td><td>(1) LSI, IC lead width is more than 50% beyond pad outline.
(2) More than 50% of LSI, IC leads is off the pad outline.</td><td>Minor</td></tr>
<tr><td>15) Conductive foreign matter (solder ball, solder hips)</td><td>(1) 0.45<Φ, N≥1
(2) 0.3<Φ≤0.45, N≥1
Φ: Average diameter of solder ball (unit: mm)
(3) 0.5<L, N≥1
L: Average length of solder chip (unit: mm)</td><td>Major
Minor

Minor</td></tr>
<tr><td>16) PCB pattern damage</td><td>(1) Deep damage is found on copper foil and the pattern is nearly broken.
(2) Damage on copper foil other than 1) above</td><td>Major
Minor</td></tr>
<tr><td>17) Faulty PCB correction</td><td>(1) Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair;2 or more places are corrected per PCB.
(2) Short-circuited part is cut, and no resist coating has been performed.</td><td>Minor</td></tr>
<tr><td>18) Bezel flaw</td><td>Bezel claw missing or not bent</td><td>Minor</td></tr>
<tr><td>19) Indication on name plate (sampling indication label)</td><td>(1) Failure to stamp or label error, or not legible.(all acceptable if legible)
(2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.</td><td>Minor</td></tr>
</table>

7.Reliability

7-1 Lifetime

50,000 hours (25℃ in the room without ray of sun)

7-2 Items of reliability

Item	Condition	Criterion
1) High Temperature Operating	60℃ 96hrs	No cosmetic failure is allowable. Contrast ratio should be between initial value ± 10%. Total current consumption should be below double of initial value.
2) Low Temperature Operation	-20℃ 96hrs	
3) Humidity	40℃, 90%RH, 96hrs	No cosmetic failure is allowable. Contrast ratio should be between initial value ± 20%. Total current consumption should be below double of initial value.
4) High Temperature	70℃ 96hrs	
5) Low Temperature	-30℃ 96hrs	
6) Thermal shock	25℃→30℃→25℃→70℃ 5(min) 30(min) 5(min) 30(min) 5 cycle, 55~60%RH	
7) Vibration	10~55~10hz amplitude: 1.5mm 2hrs for each direction (X,Y,Z)	No defects in cosmetic and operational function are allowable. Total current consumption should be below double of initial value.

8.Handling Precautions

8-1 Mounting method

A panel of LCD module consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB).

Extreme care should be used when handling the LCD modules.

8-2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- □ Isopropyl alcohol
- □ Ethyl alcohol
- □ Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- □ Water
- □ Ketone
- □ Aromatics

8-3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

8-4 Packaging

- Module employs LCD elements, and must be treated as such.
  Avoid intense shock and falls from a height.
  To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

8-5 Caution for operation

- It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.
  An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

8-6 Storage

In the case of storing for a long period of time, the following ways are recommended:

- Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.
- Storing with no touch on polarizer surface by any thing else.

8-7 Safety

- It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.

9.Precautions for Use

9-1 Both parties should provide a limit sample on an occasion when both parties agree its necessity.
The judgement by a limit sample shall take effect after the limit sample has been established and confirmed by both parties

9-2 On the following occasions, the handling of problem should be decided through discussion and agreement between responsible of the both parties.

-When a question is arisen in this manual.
-When a new problem is arisen which is not specified in this manual.
-Some problem is arisen due to the change of inspection and operating conditions in users.
-When a new problem is arisen at the customer’s operating set for sample evaluation in the customer site.