APPROVAL SHEET

Customer	:	
Part Name	:	**LCD MODULE**
Model NO.	:	**EDM2004-01**
Drawing NO.	:	
Approved by	:	
Date	:	**2006. 01.23**

Dalian Dongfu Color Display Co., Ltd.

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1. Scope

This manual defines general provisions as well as inspection standards for standard LCD module supplied by Dalian Dongfu Color Display Co., Ltd.

If the event of unforeseen problem or unspecified items may occur, please contact the nearest supplier or our company.

2. Warranty

If module is not stored or used as specified in this manual, it will be void the 12- month warranty.

3. Features

3-1. Features

Display mode: Transflective and positive type
STN LCD

Display color: Display dots: dark blue
Background: Yellow Green

Controller: S6A0075

Input data: 8-bit parallel data interfaced from a MPU

Multiplex ratio: 1/16 Duty

Viewing direction: 6 O'clock

CGROM Capacity: Character font 5×8 dots:160 characters

CGRAM Capacity: Character font 5×8 dots:8 characters

3-2. Mechanical features

Item	Specifications	Unit
Outline dimensions	98.0(W)×60.0(H)×14.5 Max.(T)	mm
Viewing Area	78.0(W)×25.0(H)	mm
Image Area	70.4(W)×20.8(H)	mm
Character Size	2.95(W)×4.75(H)	mm
Distance between characters	3.55(W)×5.35(H)	mm
Dot Size	0.55(W)×0.55(H)	mm
Dot Pitch	0.6(W)×0.6(H)	mm
Weight		g

3-3. Absolute maximum ratings

Item		Symbol	Min.	Max.	Unit	Note
Supply Voltage	Logic	Vdd	-0.3	7.0	V	1),2)
	LCD drive	Vdd – V0	Vdd-15.0	Vdd+0.3	V	1),2)
Input voltage		Vi	-	Vdd	V	1),2)
Operating Temperature		Top	-10	60	℃	
Storage Temperature		Tstg	-20	70	℃	

Note

1) The modules may be destroyed if they are used beyond absolute maximum ratings. In ordinary

operation, it is desirable to use them within recommended operation conditions. Using the modules beyond these

2) conditions may cause malfunction and poor reliability.

3) All voltage values are referenced to GND=0V.

3-4 Electrical characteristics

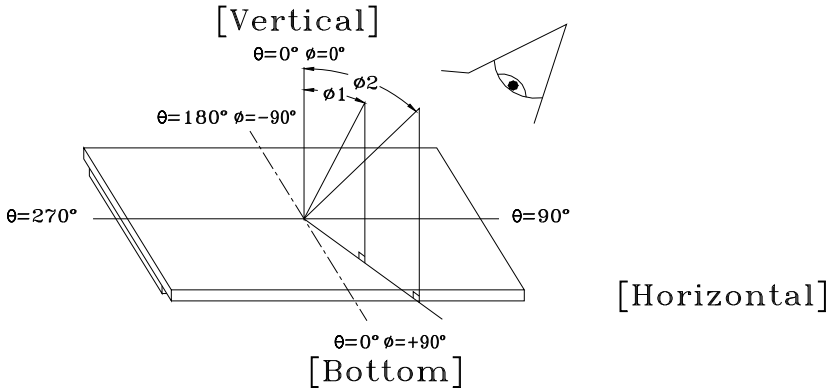
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Voltage	Logic	Vdd		4.5	5.0	6.0	V
	LCD drive	Vdd–Vee		—	5.0	—	
Input Voltage	'H' Level	Vih		0.7Vdd	—	Vdd	
	'L' Level	Vil		-0.3	—	0.55	
Output Voltage	'H' Level	Voh	-Ioh=1mA	0.75Vdd	—	—	
	'L' Level	Vol	Iol=1mA	—	—	0.2Vdd	
Internal Clock (external Rf)		Fosc	Rf=91kΩ±2%	190	270	350	KHz
Power Consumption		Idd		—	1.2	1.4	mA

Note： All the dots are in the static state.

3-5 Electro-optical Characteristics

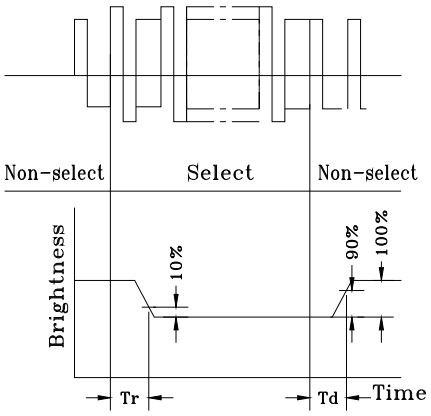
Item		Symbol	Temp.	Condition	Min.	Typ.	Max.	Unit	Note
LCD Driving Voltage (Recommended Voltage)		Vop	25℃	Φ=0°, θ=0°	—	5.0	—	V	1,2,5
Response Time	Rise Time	tr	-20℃	Φ=0°, θ=0°	—	1500	2000	mS	Response Time
			25℃		—	150	200		
	Decay Time	td	-20℃		—	3000	3500		
			25℃		—	200	250		
Viewing Angle		Δ Φ	25℃	Vertical	-35	—	35	deg.	1,4,5
				Horizontal	-30	—	30		
Contrast Ratio		K	25℃	Φ=0°, θ=0°	2.0	5.0	—	—	1,5,6

Note：<1> Definition of Φ and θ <2> Contrast ratio higher than 2(k≥2) can obtained in this voltage range.



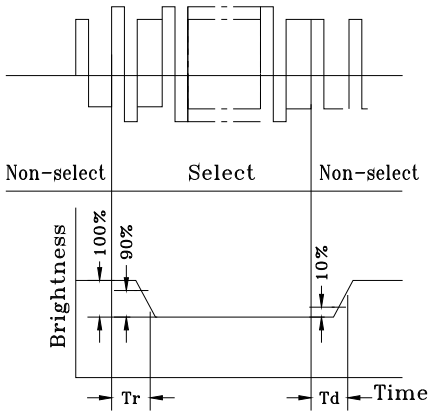
Note：<3> Definition of response time wave form

Positive Display Negative Display

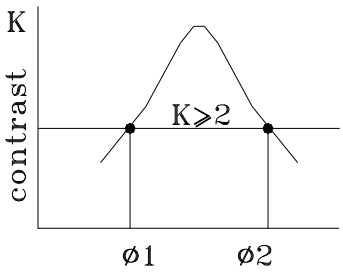


Note：<4>Definition of viewing angle

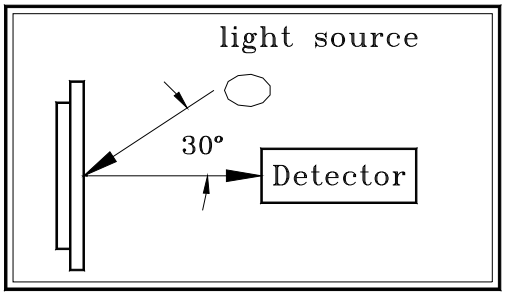
(Δ Φ) Δ Φ=|Φ1-Φ2|



Note：<5> Optical measuring system temperature regulated chamber



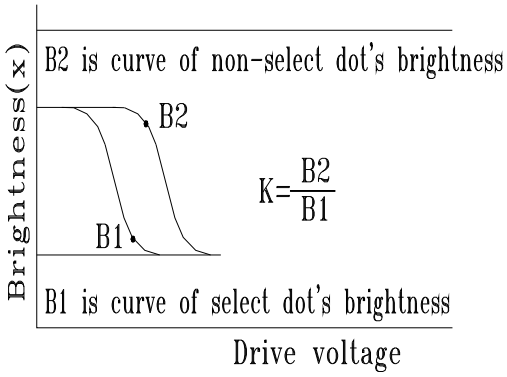
Viewing angle



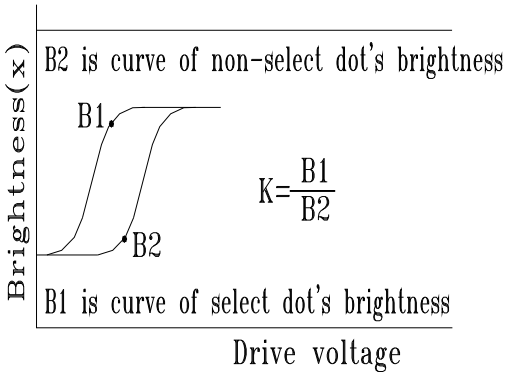
Measuring equipment: DMS
(Made in AUTRONIC)

Note：<6> Definition of contrast ratio (K)

Positive Display



Negative Display



$$\text{Contrast ratio (K)} = \frac{\text{Brightness of non-selected dot (B2)}}{\text{Brightness of selected dot (B1)}}$$

3-6 Electro-optical Characteristics of Backlight

Item	Symbol	Min.	Type	Max.	Unit	Condition
Forward Voltage	Vf		5.0		V	If=20X4mA
Reverse Current	If			200	uA	Vr=8V
Luminance	Lv	25	35		Cd/m²	If=20X4mA
Operating temperature range	Topr		-30~+70		℃	
storage temperature range	Tstg		-30~+80		℃	

4. I/O Terminal

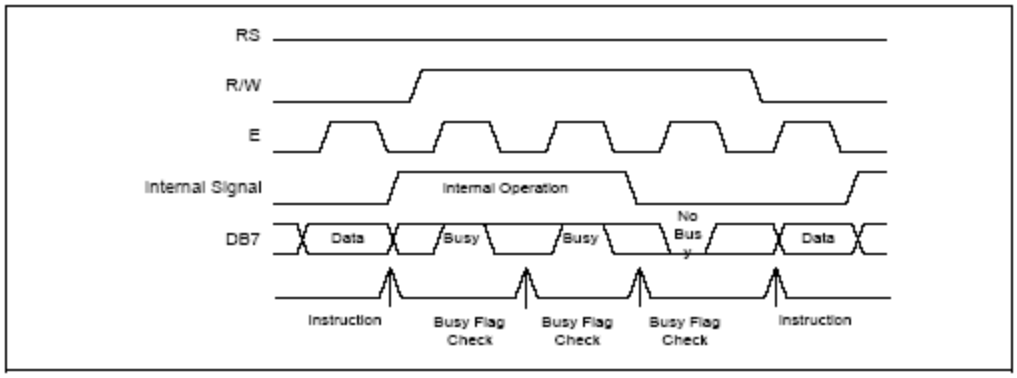
4-1. I/O Connection

Pin No.	Symbol	Function
1	Vss	Signal ground (GND)
2	Vdd	Power supply voltage (+5V)
3	Vee	Power supply for driving LCD (variable)
4	RS	Input terminal, interfaced with MPU Selects registers RS=0, Instruction register (for write) Busy flag: address counter (for read) RS=1, Data register (for write and read)
5	R/W	Input terminal, interfaced with MPU Selects read or write R/W=1 Read ； R/W=0 Write
6	E	Input terminal, interfaced with MPU The enable signal.
7~10	DB0~DB3	When 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode or serial mode, open these pins.
11~14	DB4~DB7	When 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for busy flag output. During serial mode, open these pins.

4-2 Signal timing diagram

Interface with 8-bit MPU

If 8-bit MPU is used, S6A0075 can connect directly with that. In this case, port E, RS, R/W and DB0 - DB7 need to interface each other. Example of timing sequence is shown below.

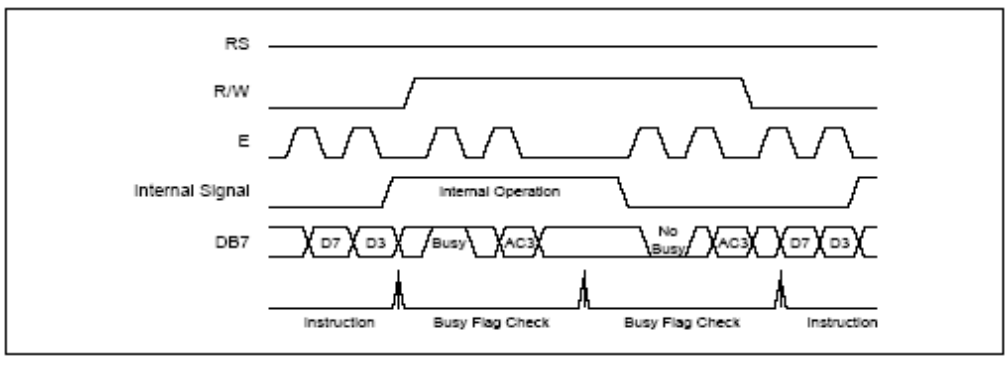


Example of 8-bit Bus Mode Timing Sequence

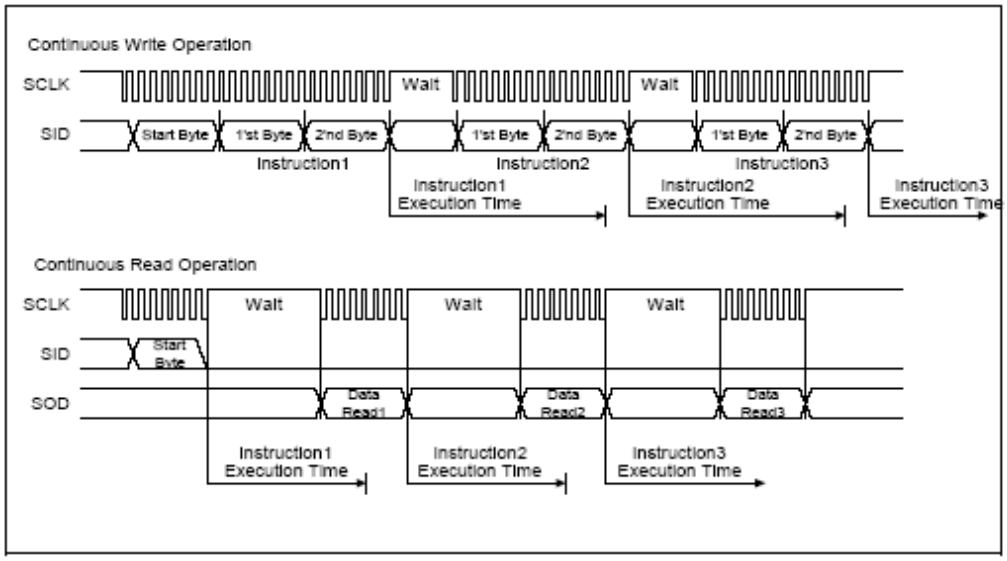
Interface with 4-bit MPU

If 4-bit MPU is used, S6A0075 can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need

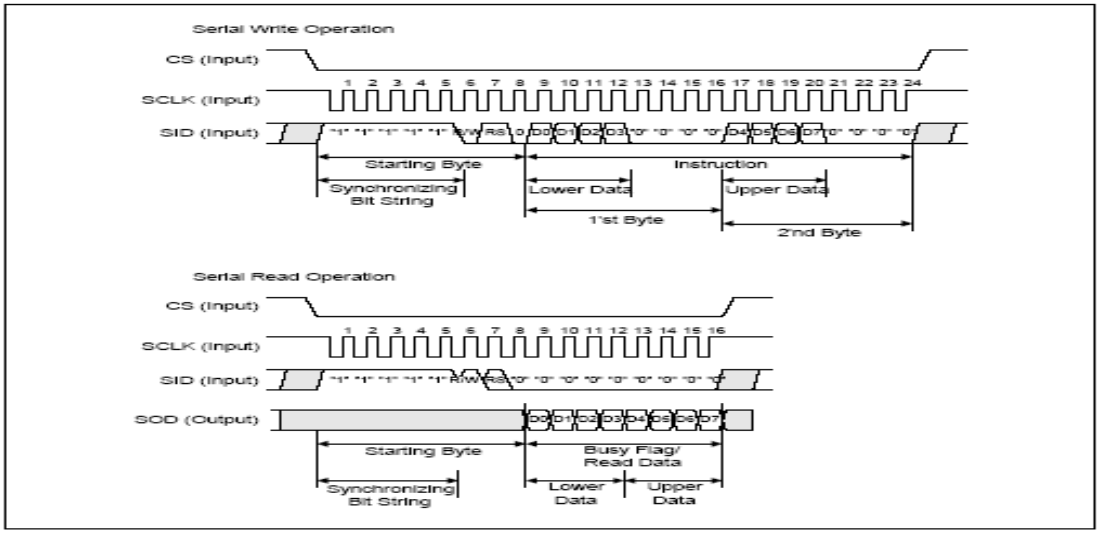
to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.



Example of 4-bit Bus Mode Timing Sequence



Timing Diagram of Serial Data Transfer



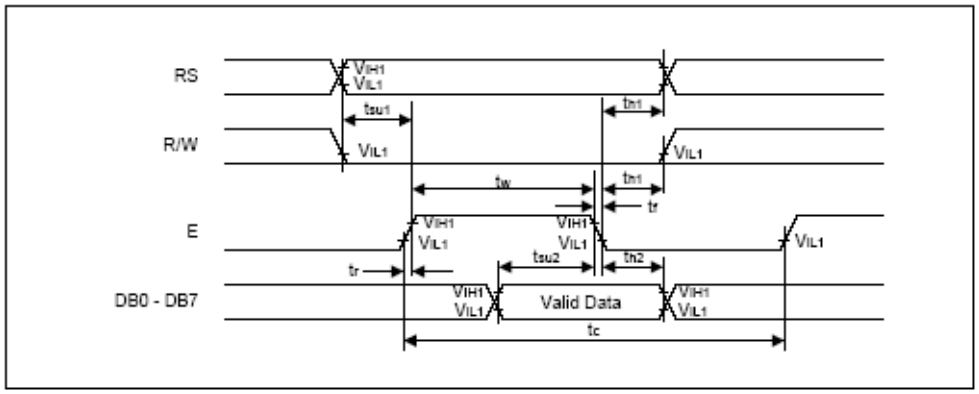
Timing Diagram of Continuous Data Transfer

AC CHARACTERISTICS (VDD = 4.5 to 5.5V, Ta = -30 to +85°C)

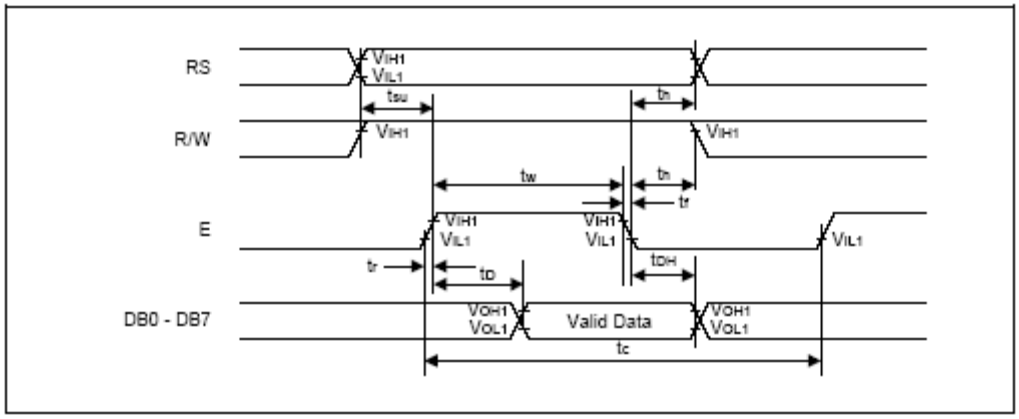
AC Characteristics

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write mode (refer to Figure15)	E cycle time	tc	500	-	-	ns
	E rise/fall time	tr, tf	-	-	20	
	E pulse width (high, low)	tw	230	-	-	
	R/W and RS setup time	tsu1	40	-	-	
	R/W and RS hold time	th1	10	-	-	
	Data setup time	tsu2	60	-	-	
	Data hold time	th2	10	-	-	
(2) Read mode (refer to Figure 16)	E cycle time	tc	500	-	-	ns
	E rise/fall time	tr, tf	-	-	20	
	E pulse width (high, low)	tw	230	-	-	
	R/W and RS setup time	tsu	40	-	-	
	R/W and RS hold time	th	10	-	-	
	Data output delay time	t_D	-	-	160	
	Data hold time	t_{DH}	5	-	-	
(3) Serial interface mode (refer to Figure 17)	Serial clock cycle time	tc	0.5	-	20	µs
	Serial clock rise/fall time	tr, tf	-	-	50	ns
	Serial clock width (high, low)	tw	200	-	-	
	Chip select setup time	tsu1	60	-	-	
	Chip select hold time	th_1	20	-	-	
	Serial input data setup time	tsu2	100	-	-	
	Serial input data hold time	th2	100	-	-	
	Serial output data delay time	t_D	-	-	160	
	Serial output data hold time	t_{DH}	5	-	-	

Mode	Item	Symbol	Min	Typ	Max	Unit
(4) Write mode (refer to Fig-15)	E cycle time	tc,	1000	-	-	ns
	E rise / fall time	tr, tf	-	-	25	
	E pulse width (high, low)	tw	450	-	-	
	R/W and RS setup time	tsu1	60	-	-	
	R/W and RS hold time	th1	20	-	-	
	Data setup time	tsu2	195	-	-	
	Data hold time	th2	10	-	-	
(5) Read mode (refer to Figure 16)	E cycle time	tc	1000	-	-	ns
	E rise/fall time	tr, tf	-	-	25	
	E pulse width (high, low)	tw	450	-	-	
	R/W and RS setup time	tsu	60	-	-	
	R/W and RS hold time	th	20	-	-	
	Data output delay time	t_D	-	-	360	
	Data hold time	t_{DH}	5	-	-	
(6) Serial interface mode (refer to Figure 17)	Serial clock cycle time	tc	1	-	20	µs
	Serial clock rise/fall time	tr, tf	-	-	50	ns
	Serial clock width (high, low)	tw	400	-	-	
	Chip select setup time	tsu1	60	-	-	
	Chip select hold time	th1	20	-	-	
	Serial input data setup time	tsu2	200	-	-	
	Serial input data hold time	th2	200	-	-	
	Serial output data delay time	t_D	-	-	360	
	Serial output data hold time	t_{DH}	5	-	-	

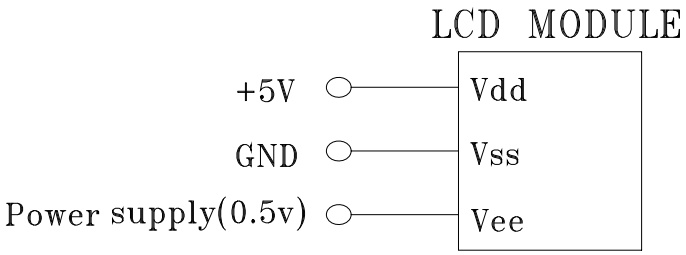


Write Mode



Read Mode

4-3 Power Supply Diagram



Descriptions for hardware and software

4-5-1 The internal structure of a module

A module consists of LCD panel, controller, segment driver(s), and bias generator circuit.

The EDM2004-01 is a character dot matrix module of 5x7 dots with cursor line, four lines, 20x4 characters.

The suitable segment driver(s) is used together with controller. It receives oscillation, alternated signal, data and shift/latch clock, to drive segment to display. Controller receives instructions and data from MPU to control the operation of module. Under the control of controller, MPU is interfaced with E, R/W, and RS by 8-bit or 4-bit data bus line DB0 to DB7, which are in the coordination in accordance with specified timing. So, by receiving the instructions and data from data bus lines, the controller finds the character codes in CGROM which are then to be put into DDRAM, and display characters in the specified positions on the LCD panel corresponding to the addresses in DDRAM. It can also realize the characters displaying, blinking, and shifting and other results by the instructions of MPU.

The controller is composed of Instruction Register (IR), Data Register (DR), Busy Flag (BF), Address Counter (AC), DDRAM, CGROM, CGRAM and Timing Generator Circuit.

FUNCTION DESCRIPTION

SYSTEM INTERFACE

This chip has all three kinds interface type with MPU: serial, 4-bit bus and 8-bit bus. Serial and bus (4-bit/8-bit) is selected by IM input, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. During read or

write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation ,reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the

next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/SEGRAM automatically. The Instruction register (IR) is used

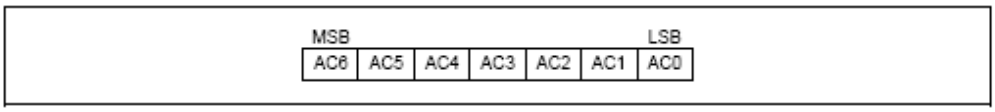
only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS/CS input pin in 4-bit/8-bit bus mode (IM = "High") or RS bit in serial mode (IM = "Low").

BUSY FLAG (BF)

RS	R/W	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation),through DB7. Before executing the next instruction, be sure that BF is not high.

DISPLAY DATA RAM (DDRAM)DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

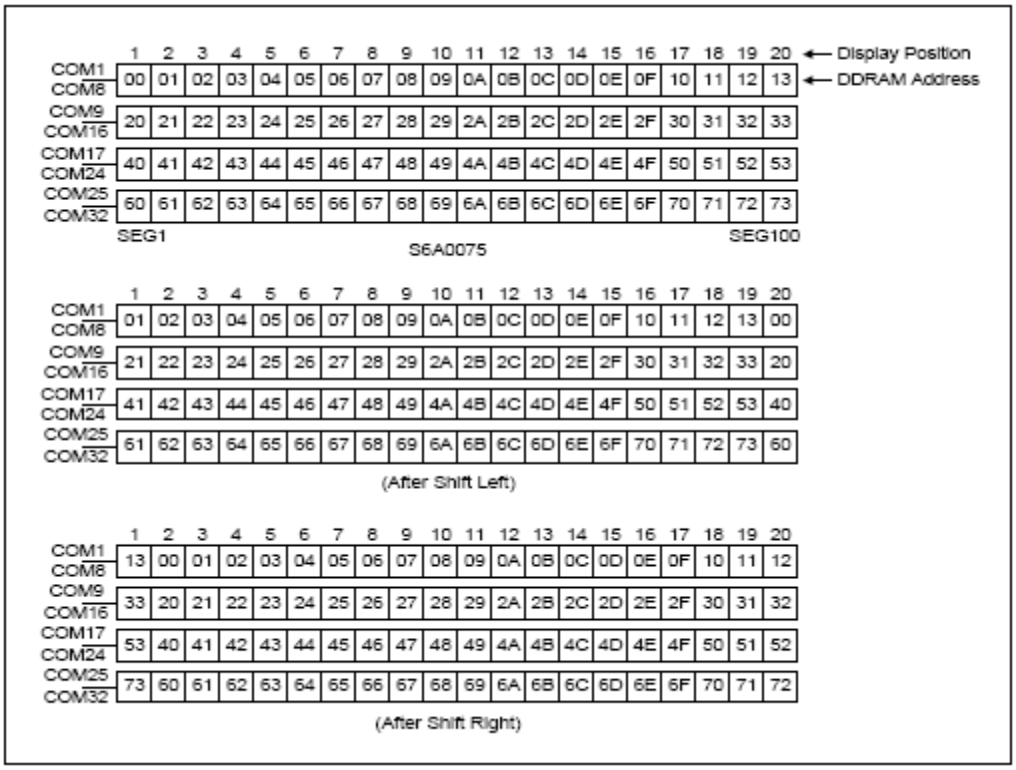


DDRAM Address

Display of 5-Dot Font Width Character

5-dot 4-line Display

In case of 4-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H -53H, 60H-73H



4-line x 20ch. Display (5-dot Font Width)

TIMING GENERATION CIRCUIT

Timing generation circuit generates clock signals for the internal operations.

ADDRESS COUNTER (AC)

Address Counter(AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W ="High", AC can be read through DB0-DB6

CURSOR/BLINK CONTROL CIRCUIT

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

LCD DRIVER CIRCUIT

LCD Driver circuit has 34 common and 100 segment signals for LCD driving. Data from SEGRAM/CGRAM/CGROM is transferred to 100-bit segment latch serially, and then it is stored to 100-bit shift latch. When each com is selected by 34-bit common register, segment data also output through segment driver from 100-bit segment latch. In case of 1-line display mode, COM0-COM17 have 1/17 duty, and in 2-line or 4-line mode, COM0-COM33 have 1/33 duty ratio.

CGROM (CHARACTER GENERATOR ROM)

CGROM has 5 × 8 dots 240 Character Pattern

CGRAM (CHARACTER GENERATOR RAM)

CGRAM has up to 5 × 8 dots 8 characters. By writing font data to CGRAM, user defined character can be used(refer to Table 4).

4 × 8 dots Character Pattern

Relationship between Character Code(DDRAM) and Character Pattern(CGRAM)

Character Code (DDRAM data)								CGRAM Address			CGRAM Data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	x	0	1	1	1	0	Pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	x	1	0	0	0	1	Pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of S6A0075 and MPU clock, S6A0075 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 6/10) Instruction can be divided largely four kinds,

- S6A0075 function set instructions (set display methods, set data length, etc.)
- Address set instructions to internal RAM
- Data transfer instructions with internal RAM
- Others .

The address of internal RAM is automatically increased or decreased by 1.

When IE = "High", S6A0075 is operated according to instruction set 1

and when IE = "Low", S6A0075 is operated according to instruction set 2 .

NOTE: During internal operation, busy flag (DB7) is read high. Busy flag check must precede the next instruction. When an MPU program with Busy Flag (DB7) checking is made, 1/2 fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

INSTRUCTION DESCRIPTION 1 (IE = "HIGH")

Instruction Set 1

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Power down mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD = "1":power down mode set, PD = "0":power down mode disable	39μs
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1": increment, I/D = "0": decrement and display shift enable bit. S = "1": make display shift of the enabled lines by the DS4 DS1 bits in the shift enable instruction. S = "0": display shift disable	39μs
	1	0	0	0	0	0	0	0	1	1	B/D	Segment bi-direction function. BID = "0": Seg1 → Seg80, BID = "1": Seg80 → Seg1.	
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1": display on, D = "0": display off, C = "1": cursor on, C = "0": cursor off, B = "1": blink on, B = "0": blink off.	39μs

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width, B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable NW = "1": 4-line display mode, NW = "0": 1-line or 2-line display mode.	39μs
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	x	x	Cursor or display shift. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left.	39μs
Shift Enable	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(when DH = "1") Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.	39μs
Scroll enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH = "0") Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.	39μs

NOTES:

1. When an MPU program with busy flag (DB7) checking is made, 1/2 fosc (is necessary) for executing the next instruction by the "E" signal after the busy flag (DB7) goes to "Low"
2. "X": Don't care

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home: (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Power Down Mode Set: (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction. When PD = "High", it makes S6A0075 suppress current consumption except the current needed for data storage by executing next three functions.

- Make the output value of all the COM/SEG ports VDD
- Make the COM/SEG output value of extension driver VDD by setting D output to "High" and M output to "Low"
- Disable voltage converter to remove the current through the divide resistor of power supply.

You can use this instruction as power sleep mode.

When PD = "Low", power down mode becomes disabled.

Entry Mode Set

(RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

- CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 - DS4 bits in the shift enable instruction is shifted to the right (I/D = "0") or to the left (I/D = "1"). But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display like this function is not performed.

(RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set.

BID: Data shift direction of segment.

When BID = "Low", segment data shift direction is set to normal order from SEG1 to SEG100.

When BID = "High", segment data shift direction is set to reverse from SEG100 to SEG1.

By using this instruction, you can raise the efficiency of application board area.

- The BID setting instruction is recommended to be set at the same time level of function set instruction.
- DB1 bit must be set to "1".

Display ON / OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit

When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270kHz frequency, blinking has 370 ms interval. When B = "Low", blink is off.

Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	B/W	NW

FW: Font Width control

When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.

The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0, including the left most space bit of CGRAM.

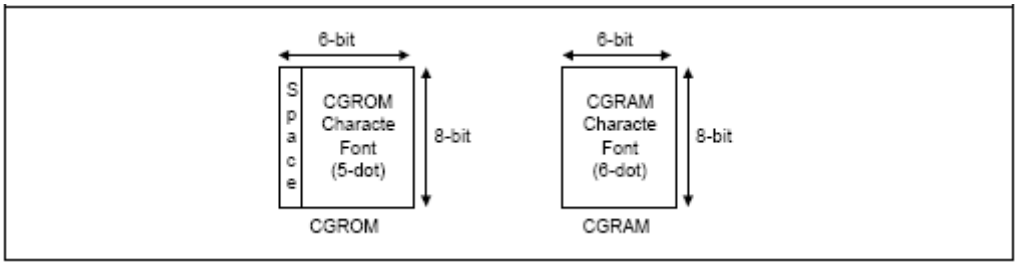
When FW = "Low", 5-dot font width is set.

B/W: Black/White Inversion enable bit

When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270kHz, inversion has 370 ms intervals.

NW: 4 Line mode enable bit

When NW = "High", 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.



6-dot Font Width CGROM/CGRAM

Cursor or Display Shift (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

Shift right/left cursor position or display, without writing or reading of display data, this instruction is use to correct or search display data (refer to Table 7). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. When 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note

that display shift is performed simultaneously in all the line enabled by DS1-DS4 in the shift enable instruction. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are changed. During low power consumption mode, display shift may not be performed normally.

Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Shift/Scroll Enable (RE = 1)

(DH = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS: Horizontal scroll per line enable

This instruction makes valid dot shift by a display line unit. HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line. If you want to scroll the line in 1-line display mode or the 1st line in 2-line display mode, set HS1 and HS2 to "High". If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High".

(DH = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS: Display shift per line enable this instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.

If you set DS1 and DS2 to "High" (enable) in 2 line mode, only the 1st line is shifted and the 2nd line is not shifted. When only DS1 = "High", only the half of the 1st line is shifted. If all the DS bits (DS1 to DS4) are set to "Low" (disable), no display is shifted.

Relationship between DS and COM signal

Enable Bit	Enabled Common Signals During Shift	Description
HS1/DS1	COM1 - COM8	The part of display line that corresponds to enabled common signal can be shifted.
HS2/DS2	COM9 - COM16	
HS3/DS3	COM17 - COM24	
HS4/DS4	COM25 - COM32	

Function Set

(RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(0)	DH	REV

DL: Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit

It is variable only when NW bit of extended function set instruction is low.

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.
RE: Extended function registers enable bit
At this instruction, RE must be "Low".
DH: Display shift enable selection bit.
When DH = "High", display shift per line becomes enable.
When DH = "Low", smooth dot scroll becomes enable.
This bit can be accessed only when IE pin input is "High".
REV: Reverse enable bit
When REV = "High", all the display data are reversed. Namely, all the white dots become black and black dots become white.
When REV = "Low", the display mode set normal display.
(RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE(1)	BE	0

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU.
So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.
N: Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.
RE: Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, BID bit, HS/DS bits of shift/scroll enable instruction and BE bits of function set register can be accessed.
BE: CGRAM/SEGRAM data blink enable bit
If BE is "High", It makes user font of CGRAM and segment of SEGRAM blink. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	X	X	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display

mode(N = 0, NW = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H". In 4-linedisplay mode (NW = 1), DDRAM address is from "00H" - "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" - "53H" in the 3rd line and from "60H" - "73H" in the 4th line.

Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ	SQ4	SQ3	SQ2	SQ1	SQ0

As set SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units (Refer to Table 9). In this case S6A0075 can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

Scroll Quantity According to HDS bits

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift left by 1-dot
0	0	0	0	1	0	Shift left by 2-dot
0	0	0	0	1	1	Shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	Shift left by 47-dot
1	1	X	X	X	X	Shift left by 48-dot

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether S6A0075 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM. The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data From RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

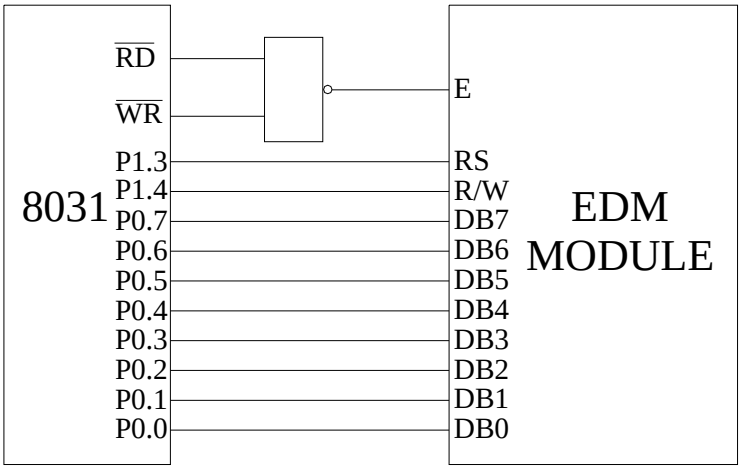
Read binary 8-bit data from DDRAM/CGRAM/SEGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data
register. After read operation address counter is automatically increased/decreased by 1 according to the

entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly. In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next

address position, but you can read only the previous data by read instruction.

The following is an application example of the module.

□ Application Circuit:



□ Application Program:

① Check the Busy Flag (BF)

```
BF：CLR    A
     CLR    RS
     SETB   R/W
     MOVX   A，@R0
     JB     ACC.7，BF
     RET
```

② Write data to IR

R1：Temporarily stores instruction code

```
WI：CLR    R/W
    CLR    RS
    MOV    A，R1
    MOVX   @R0，A
    RET
```

③ Write data to DR

R2：Temporarily stores character code or character pattern data

```
WD：SETB   RS
    CLR    R/W
    MOV    A，R2
    MOVX   @R0，A
    RET
```

④ Delay 65ms

```
DELAY：MOV    R7，#0FFH
LOOP0：MOV    R6，#0FFH
       DJNZ   R6，$
       DJNZ   R7，LOOP0
       RET
```

⑤ Write custom character pattern data to CGRAM

```
 WCG：  MOV    DPTR，#TAB
        MOV    R1，#40H
        LCALL BF
        LCALL WI
        MOV    R4，#40H          ；Character pattern data are transferred to AC.
LOOP4：CLR    A
        MOVC   A，@A+DPTR
        MOV    R2，A
        LCALL BF
        LCALL WD
        INC    DPTR
        DJNZ   R4，LOOP4
        RET
```

⑥Initializing module by instruction：

```
INI：  MOV     R3，#03H
       MOV     R1，#38H          ；Function set：8-bit data，1/16 DUTY，5X8 font
       LCALL   WI
       DJNZ    R3，INI
       MOV     R1，#01H          ；Clear display
       LCALL   BF
       LCALL   WI
       MOV     R1，#06H          ；Input mode set：AC increments by 1
       LCALL   BF
       LCALL   WI
       MOV     R1，#0CH          ；Display on
       LCALL   BF
       LCALL   WI
       RET
```

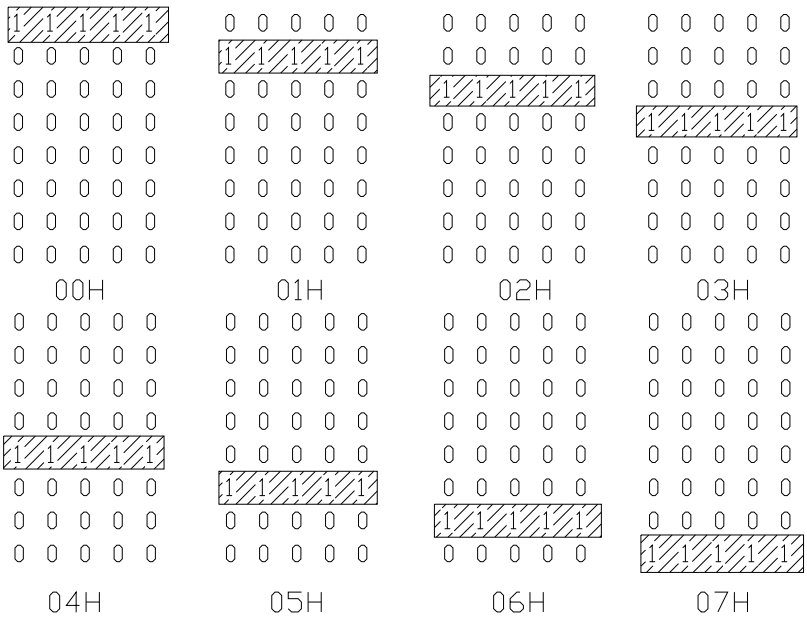
⑦ Custom character

Character pattern data group

```
TAB
DB 1FH，00H，00H，00H，00H，00H，00H，00H
DB 00H，1FH，00H，00H，00H，00H，00H，00H
DB 00H，00H，1FH，00H，00H，00H，00H，00H
DB 00H，00H，00H，1FH，00H，00H，00H，00H
DB 00H，00H，00H，00H，1FH，00H，00H，00H
DB 00H，00H，00H，00H，00H，1FH，00H，00H
DB 00H，00H，00H，00H，00H，00H，1FH，00H
```

DB 00H，00H，00H，00H，00H，00H，00H，1FH

Custom character pattern bitmap



⑧ Write displayed character codes to DDRAM：

```
WDD：  MOV    DPTR，#0300H
       MOV    R5，#11H              ；16 characters are displayed.
LOOP2：MOV    R1，#80H               ；  Display the first line and the third line.
       LCALL BF
       LCALL WI
       MOV    R3，#29H              ；Every character is displayed forty times
LOOP1：CLR    A
       MOVC   A，@A+DPTR
       MOV    R2，A
       LCALL BF
       LCALL WD
       DJNZ   R4，LOOP1
       MOV    R1，#0C00H            ；Display the second line and the fourth line
       LCALL BF
       LCALL WI
LOOP3: CLR    A
       MOVC   A，@A+DPTR
       MOV    R2，A
       LCALL BF
       LCALL WD
       DJNZ   R4，LOOP3
       RET
```

⑨ Character codes for displayed characters：

```
ORG 0300H
DB 00H，01H，02H，03H，04H，05H，06H，07H
DB 06H，05H，04H，03H，02H，01H，00H，38H
```

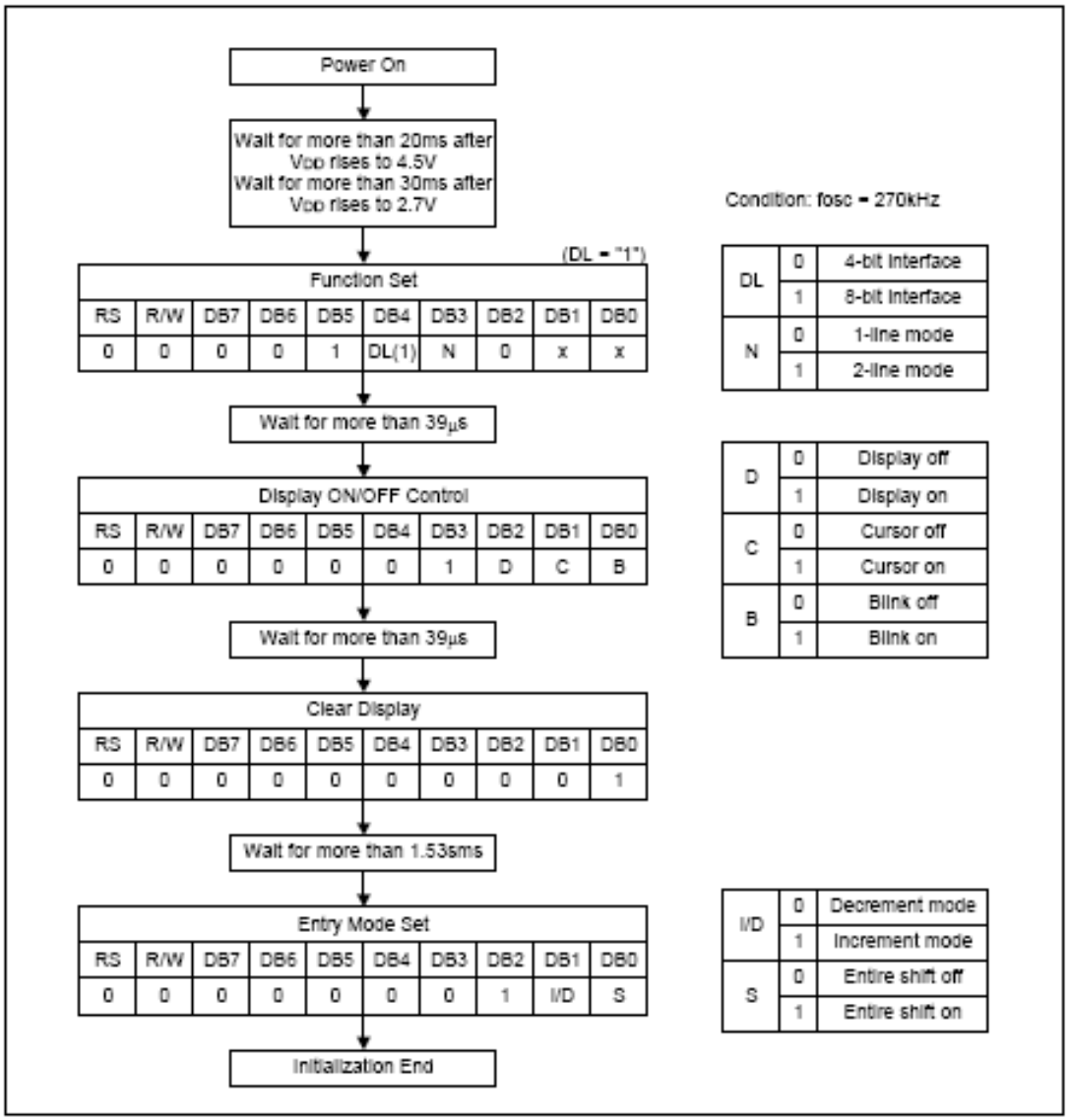
⑩ Main program for display

```
START:RS   EQU   P1.3
```

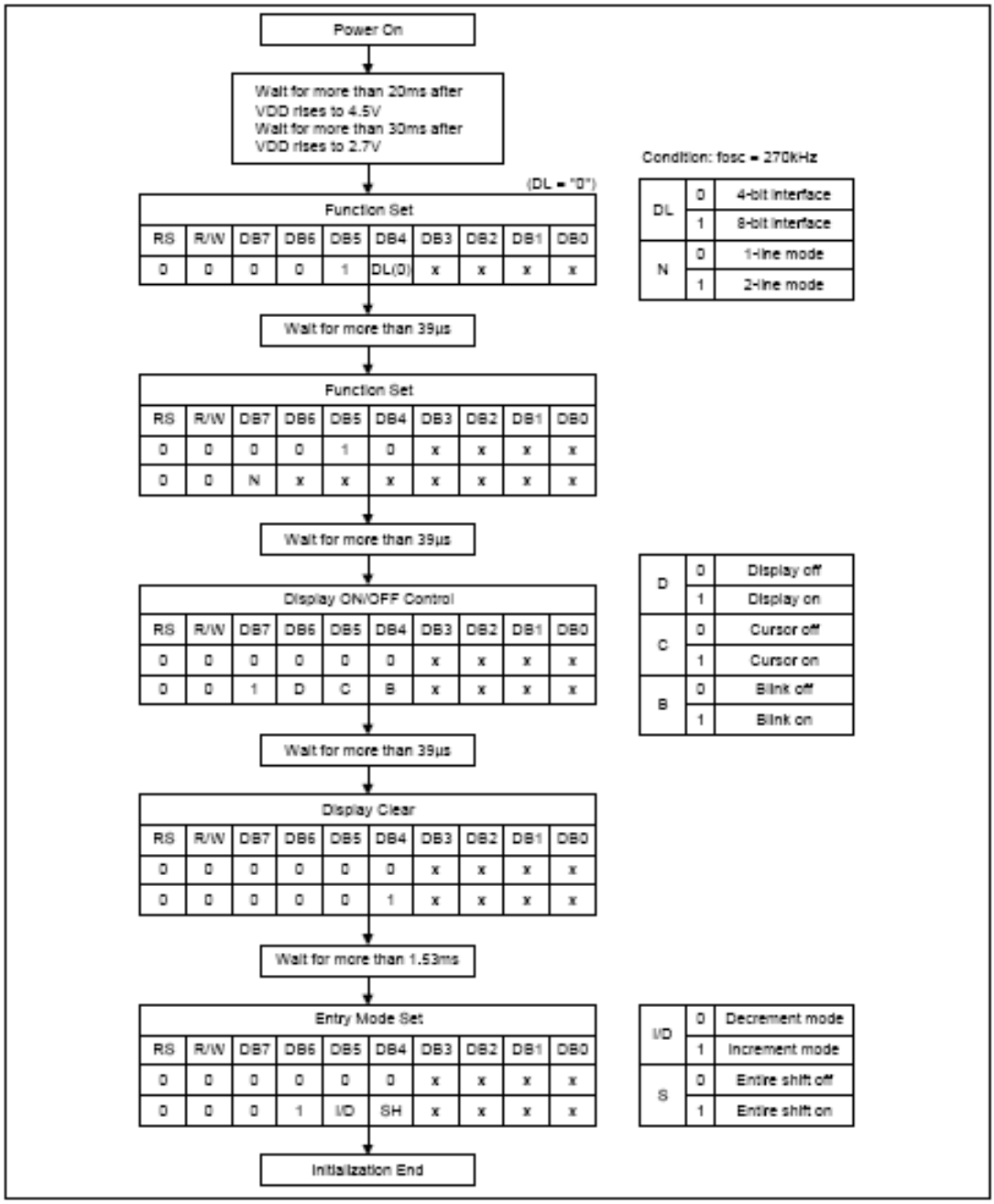
```
R/W EQU  P1.4
ORG 0000H
LCALL INI
LCALL WCG
LCALL WDD
LCALL DELAY
LCALL DELAY
LJMP START
```

The flow chart for display program

8-BIT INTERFACE MODE



4-BIT INTERFACE MODE



5.Handling precautions

5-1 Mounting method

A panel of LCD module made by Dalian Eastern Display Co., Ltd. consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB).

Extreme care should be used when handling the LCD modules.

5-2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- □ Isopropyl alcohol
- □ Ethyl alcohol
- □ Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- □ Water
- □ Ketone
- □ Aromatics

5-3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

5-4 Packaging

- Module employs LCD elements, and must be treated as such.
  Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

5-5 Caution for operation

- It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.
  An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

5-6 Storage

In the case of storing for a long period of time, the following ways are recommended:

- Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.
- Storing with no touch on polarizer surface by any thing else.

5-7 Safety

- It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.

6.Precaution for use

6-1 Both parties should provide a limit sample on an occasion when both parties agree its necessity. The judgement by a limit sample shall take effect after the limit sample has been established and confirmed by both parties

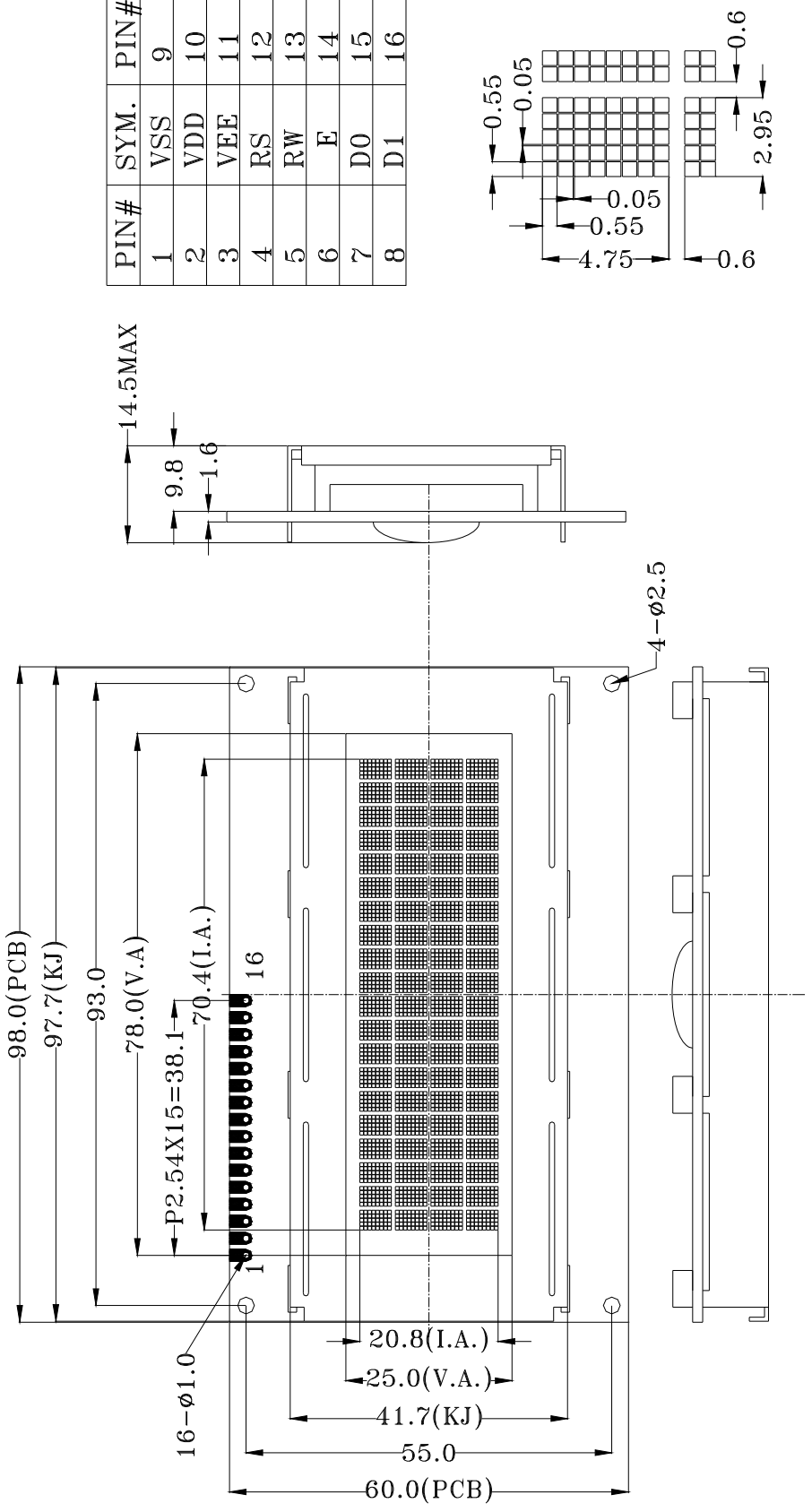
6-2 On the following occasions, the handling of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this manual.
- When a new problem is arisen which is not specified in this manual.
- Some problem is arisen due to the change of inspection and operating conditions in users.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

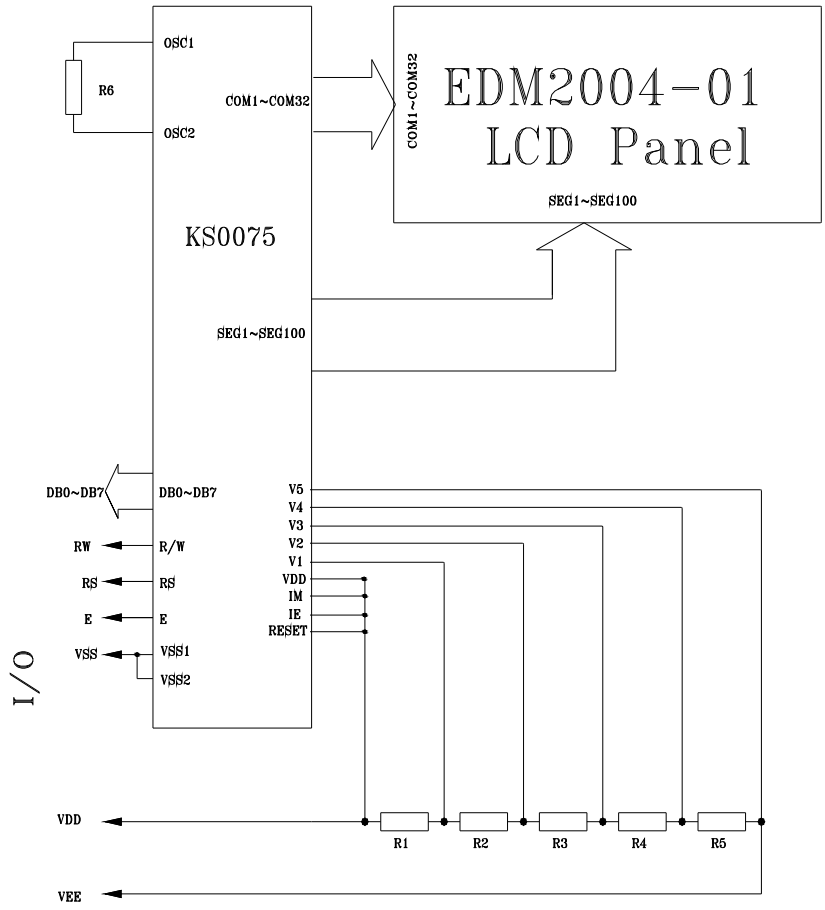
7.External Dimensions and Block Diagrams

□ External Dimensions

PIN#	SYM.	PIN#	SYM.
1	VSS	9	D2
2	VDD	10	D3
3	VEE	11	D4
4	RS	12	D5
5	RW	13	D6
6	E	14	D7
7	D0	15	BLA
8	D1	16	BLK



□ Block Diagram


OSC1
R6
OSC2
COM1~COM32
KS0075
SEG1~SEG100
COM1~COM32
EDM2004-01
LCD Panel
SEG1~SEG100
DB0~DB7
DB0~DB7
RW
R/W
RS
RS
E
E
VSS
VSS1
VSS2
I/O
V5
V4
V3
V2
V1
VDD
IM
IE
RESET
VDD
VEE
R1
R2
R3
R4
R5